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INSPEC - 1969 to date (INZZ)

Accession number & update
8031736, B2004-08-2210B-007; 20040718.

Title
Analysis and **measurement** of small **inductance** of loops and vias on printed circuit board.

Author(s)
Yang-Chen; Guozhu-Chen; Smedley-K.

Author affiliation
Dept of Electr Eng & Comput Sci, California Univ, Irvine, CA, USA.

Source
IECON'03. 29th Annual Conference of the IEEE Industrial Electronics Society, Vol.2, Roanoke, VA, USA, 2-6 Nov. 2003.
Sponsors: IEEE Industrial Electronics Soc.
In: p.1661-6 Vol.2, 2003.

ISSN
ISBN: 0-7803-7906-3, CCCC: 0-7803-7906-3/03/ ($17.00).

Publication year
2003.

Language
EN.

Publication type
CPP Conference Paper.

Treatment codes
T Theoretical or Mathematical; X Experimental.

Abstract
Printed circuit board (PCB) design has become a crucial issue for high density packaging of power electronics circuits. The traces, loops and vias on the PCB all introduce **parasitic inductance,** which causes high frequency ringing in the circuit and thus additional losses. In this paper, the **inductance** of several typical loops and vias on PCB is analyzed using Neumann formula. Studies show that the **self-**

inductance of the rectangular loop is related to the length/width ratio, the trace width as well as the rectangular area. The mutual **inductance** between two loops is related to their relative position as well as their common area. When a loop contains vias, they may introduce additional **inductance** due to the additional cross-sectional area formed by the vias, while the vias themselves have little contribution to the **inductance** in the switching frequency domain. A simple and accurate test circuit was built based on oscillation method to measure the small **inductance** of loops on the PCB. Experimental results match the theoretical prediction with acceptable errors. Finally, some useful design guidelines are presented to optimize the layouts. (6 refs).

Descriptors

circuit-oscillations; inductance-measurement; power-electronics; printed-circuit-design.

Keywords

printed circuit board design; high density packaging; power electronics circuits; traces; loops; vias; oscillation method; **inductance measurement;** Neumann formula.

Classification codes

B2210B (Printed circuit layout and design).
B2560P (Power semiconductor devices).
B2570P (Power integrated circuits).
B7310J (Impedance and admittance **measurement**).

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INSPEC - 1969 to date (INZZ)

Accession number & update

6996465, B2001-09-7310J-004; 20010730.

Title

Characteristic-impedance **measurement** error on lossy substrates.

Author(s)

Williams-D-F; Arz-U; Grabinski-H.

Author affiliation

Nat Inst of Stand & Technol, Boulder, CO, USA.

Source

IEEE-Microwave-and-Wireless-Components-Letters (USA), vol.11, no.7, p.299-301, July 2001. , Published: IEEE.

CODEN

IMWCBJ.

ISSN

ISSN: 1531-1309, CCCC: 1531-1309/2001/ ($10.00).

Availability

SICI: 1531-1309(200107)11:7L.299:CIME; 1-Z
Electronic Journal Document Number: S1531-1309(01)05937-2.

Publication year

2001.

Language

EN.

Publication type

J Journal Paper.

Treatment codes
T Theoretical or Mathematical.
Abstract
This paper examines error caused by **parasitic inductance** in the characteristic impedance measured by the calibration comparison method on lossy silicon substrates. (13 refs).
Descriptors
calibration; electric-impedance-measurement; measurement-errors; microwave-measurement.
Keywords
characteristic impedance **measurement** error; **parasitic inductance;** calibration comparison method; lossy silicon substrate; Si.
Classification codes

```
B7310J    (Impedance and admittance measurement).
B7310N    (Microwave measurement techniques).
B7130     (Measurement standards and calibration).
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Chemical indexing
Si sur, Si el.
Copyright statement

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INSPEC - 1969 to date (INZZ)

Accession number & update
5409621, B9612-7310J-006; 961029.
Title
Nanohenry **inductance measurement** using a low **parasitic-inductance** probe.
Author(s)
Shimizu-H; Nagata-T; Nakamura-A.
Author affiliation
Mech Eng Res Lab, Hitachi Ltd, Tsuchiura, Japan.
Source
Electronics-and-Communications-in-Japan-Part-2 (Electronics)(USA), vol.79, no.6, p.95-102, June 1996. , Published: Scripta Technica.
CODEN
ECJEEJ.
ISSN
ISSN: 8756-663X, CCCC: 8756-663X/96/0006-0095.
Availability
SICI: 8756-663X(199606)79:6L.95:NIMU; 1-Q.
Publication year
1996.
Language
EN.
Publication type
J Journal Paper.
Treatment codes
P Practical; X Experimental.
Abstract
The increased speeds of logic circuitry make the electrical characteristics of LSI packages more

important. This is especially true of **inductance,** which is the main source of simultaneous switching noise (SSN). To improve the accuracy of SSN simulations, **inductance** models of LSI packages should be represented by **inductance** matrices, and thus to construct precise models, it is necessary to have an **inductance measurement** method. A new **inductance measurement** method of nanohenry-order accuracy is proposed that uses an LCR-meter. Since the **parasitic inductance** of **measurement** probes usually decreases accuracy, a special probe with minimized **parasitic inductance** was developed. The new **measurement** method has the additional advantage of high spatial resolution. The results of measurements proved to be in good agreement with calculations. (7 refs).

Descriptors

inductance-measurement; integrated-circuit-modelling; integrated-circuit-noise; large-scale-integration; logic-design; probes.

Keywords

inductance measurement; low **parasitic inductance** probe; logic circuitry; electrical characteristics; LSI packages; **inductance;** simultaneous switching noise; SSN simulation; **inductance** models; **inductance** matrices; LCR meter; **parasitic inductance; measurement** probes; spatial resolution.

Classification codes

B7310J (Impedance and admittance **measurement**).
B1265B (Logic circuits).
B2570A (Integrated circuit modelling and process simulation).

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INSPEC - 1969 to date (INZZ)

Accession number & update

5197808, B9604-7310J-005; 960227.

Title

Nanohenry **inductance measurement** using a **low-parasitic-inductance-** probe.

Author(s)

Shimizu-H; Nagata-T; Nakamura-A.

Author affiliation

Mech Eng Res Lab, Hitachi Ltd, Tsuchiura, Japan.

Source

Transactions-of-the-Institute-of-Electronics-Information-and-Communication-Engineers-C-II (Japan), vol.J79C-II, no.1, p.8-14, Jan. 1996. , Published: Inst. Electron. Inf. & Commun. Eng.

CODEN

DCSOEF.

ISSN

ISSN: 0915-1907.

Availability

SICI: 0915-1907(199601)J79CII:1L.8:NIMU; 1-4.

Publication year

1996.

Language

JA.

Publication type

J Journal Paper.

Treatment codes
X Experimental.
Abstract
Increasing speeds of logic systems add importance to the electrical characterization of LSI packages especially characterization of **inductance** which is a main source of simultaneous switching noise (SSN). To improve the SSM simulation accuracy, **inductance** models of LSI packages should be represented by **inductance** matrices. To construct precise **inductance** models, it is desirable to have an **inductance measurement** method. A new **inductance measurement** method of nanohenry order is proposed using an LCR meter. Since **parasitic inductance** of probes usually decreases **measurement** accuracy, we developed a special probe to minimize such **parasitic inductance.** The new **measurement** method has special merits such as high spatial resolution. The results measured were proved to be in good agreement with simulation. (9 refs).
Descriptors
inductance-measurement; probes.
Keywords
parasitic inductance; nanohenry **inductance measurement;** LSI packages; simultaneous switching noise; probe; logic systems; LCR meter; spatial resolution; simulation.
Classification codes
B7310J (Impedance and admittance **measurement).**
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INSPEC - 1969 to date (INZZ)

Accession number & update
5170139, A9604-0750-009, B9603-7310J-003; 960123.
Title
Sub-nanohenry **inductance measurement** using a **zero-parasitic-inductance** probe system.
Author(s)
Nagata-T; Shimizu-H; Nakamura-A; Fukumoto-H.
Author affiliation
Mech Eng Res Lab, Hitachi Ltd, Ibaraki, Japan.
Source
1995 Proceedings. 45th Electronic Components and Technology Conference, Las Vegas, NV, USA, 21-24 May 1995.
In: p.337-42, 1995.
ISSN
ISBN: 0-7803-2736-5, CCCC: 0569-5503/95/0000-0337 ($3.00).
Publication year
1995.
Language
EN.
Publication type
CPP Conference Paper.
Treatment codes
N New Development; P Practical; X Experimental.
Abstract
A new **inductance measurement** method of a sub-nanohenry order is proposed using an LCR meter. Since **parasitic** inductances of probes usually decreases the **measurement** accuracy, we developed two types of special probes to minimize such **parasitic** inductances. The new **measurement** methods have special merits, such as separate measurements of each trace and a high spatial resolution. They also enable measurements of inductances not only for simple traces, but also for combined trace-and-sheet conductor systems. The results measured proved to be in good agreement with our electro-magnetic simulator. The eddy current effect was successfully demonstrated by using this method. (6

refs).

Descriptors
equivalent-circuits; inductance-measurement; measurement-errors; probes.

Keywords
sub nanohenry **inductance measurement;** zero **parasitic inductance** probe system; LCR meter; **parasitic inductance** minimisation; eddy current effect.

Classification codes

A0750 (Electrical instruments and techniques).
A0620D (Measurement and error theory).
B7310J (Impedance and admittance measurement).
B7110 (Measurement theory).

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☑ **document 30 of 45** Order Document

INSPEC - 1969 to date (INZZ)

Accession number & update
4580332, B9403-0170J-004; 940120.

Title
Characterizing IC packages and interconnects.

Author(s)
Jones-K.

Author affiliation
Tektronix Inc, Beaverton, OR, USA.

Source
Test-Measurement-World (USA), vol.13, no.7, p.55-6, 58, 60, June 1993.

CODEN
TMWOD8.

ISSN
ISSN: 0744-1657.

Publication year
1993.

Language
EN.

Publication type
J Journal Paper.

Treatment codes
P Practical.

Abstract
Without question, IC packages and interconnects are the greatest obstacles to improving computer performance. Connection delays, not device speeds, are limiting the performance of today's high-speed computers. Edge speeds of digital ICs are now so fast you can no longer ignore the **parasitic inductance** and capacitance of IC interconnects. Measuring and modeling the characteristics of IC packages and interconnects will help you to increase the performance of your IC designs. (0 refs).

Descriptors
characteristics-measurement; digital-integrated-circuits; packaging.

Keywords
edge speeds; connection delays; IC packages; interconnects; computer performance; high speed

computers; digital ICs; **parasitic inductance;** capacitance.

Classification codes

B0170J (Product packaging).
B1265 (Digital electronics).

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INSPEC - 1969 to date (INZZ)

Accession number & update

43572, B69013037; 690000.

Title

Measurement of **parasitic inductance** of capacitors.

Source

Przeglad-Elektroniki (Poland), vol.10, no.1, p.42-43, 1969.

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CODEN

PRELAX.

ISSN

ISSN: 0552-4172.

Publication year

1969.

Language

PO.

Publication type

J Journal Paper.

Descriptors

capacitors; inductance; inductance-measurement.

Classification codes

B2130 (Capacitors).
B7310J (Impedance and admittance).

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